Equalizer Training in IEEE 802.11b Standard

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***Abstract*-Wireless local area networks (WLANs) have gained importance lately with the WLAN standard, IEEE 802.11b, being extensively deployed. In this paper, we present a novel training technique for a modified DFE equalizer and show that, for the CCK modulation and due to error feedback, it outperforms other equalization methods.**

I. INTRODUCTION

Wireless local area networks (WLANs) have gained importance lately. With the emergence of hotspots, many university campuses and airports are already covered by the WLAN standard, IEEE 802.11b. In this paper, we discuss an important component in deciding the performance of an 802.11b receiver, namely channel estimation and equalization. Signals in a typical 802.11b environment suffer from a multipath fading channel. This channel can be modeled as a tapped delay line. This means that at the receiver, and rather than receiving a single replica of the transmitted signal, there would be an overlap of several delayed replicas of the transmitted signal. This requires the use of channel correction in the receiver. The channel correction can be divided into two parts, the first part estimates the delays and their corresponding gains, i.e. estimating the channel. The second part would correct for the channel, which can be called equalization. Depending on the nature of the channel and the nature of the modulated signal used in the transmitter, one would choose between several channel correction options. The 802.11b standard has four modulation formats. All four of them use a symbol that is composed of several chips, either 11 in case of the 1 and 2 Mbps bit rates, or 8 chips in case of the higher 5.5 and 11 MBPS bit rates. Because of the fact that the symbols are not composed of only one chip, the equalization schemes used have to take that into account. The simplest channel corrector is the matched filter [1], where one would filter the received signal with a time-flipped replica of the estimated channel. However, this simple "equalizer", as will be shown, would only work with some of the modulation formats used in the IEEE 802.11b. Several other equalization schemes exist, some are linear and some are non-linear. In this paper we are concerned with the non-linear MMSE decision feedback (MMSE-DFE) [2] equalizer. Specifically, we will show how the 802.11b receiver performs when it uses two variants of the DFE equalizer. The first of the two variants is the classical DFE where one would feed back, through the feedback filter, estimates of the transmitted data. In the 11b signal, one would have to feedback, at each chip boundary, estimate of that chip. We call this the interchip interference based (ICI-based) DFE. Another variant is what we call an intersymbol interference (ISI) based DFE, which is only concerned with canceling the intersymbol interference. Here, one would feedback chip estimates only at the edges of the symbols rather than at the edge of each chip. However, training mechanisms used to obtain equalizer taps of the conventional DFE cannot be used for the ISI-DFE. The authors of this paper are unaware of any training mechanisms of the ISI-DFE except for the one used in [3], where the coefficients are obtained directly from the channel estimate. Theoretically, this is not the optimal DFE coefficients, In this paper, we present several training mechanisms for the ISI-DFE equalizer.

This paper is organized as follows. We begin the paper by giving a brief overview of the IEEE 802.11b standard and explaining its different modulation formats. We then introduce the channel model typically encountered in the WLAN indoor environments. In the next section we present several solutions for the equalization of an 802.11b signal. We present the ICI-based DFE and the ISI-based DFE. We then propose two techniques for obtaining the optimal coefficients of the DFE. One of these techniques is the Least Squares (LS) and the other is the adaptive Least Mean Squares (LMS). The simulation results showing the performance of these different techniques are shown. We end with the conclusion.

II. IEEE 802.11B STANDARD

There are four data rates supported by the IEEE 802.11b standard. The lower 2 rates, the 1 and 2 Mbps, use a pseudo random Barker code to spread the data. The Barker code has 11 chips, and the chip rate used is 11 Mchips per second. The 1 and 2 Mbps rates use DBPSK and DQPSK modulation respectively. The higher 2 rates, the 5.5 and 11 Mbps, use the complementary code keying (CCK) modulation [4]. This modulation uses either 16 or 256 chip sequences, each with 8 chips, to achieve 5.5 or 11 Mbps data rates respectively. Hence a CCK "symbol" is composed of 8 chips. The 5.5 Mbps maps 4 bits into one of the possible 16 symbols, and the 11 Mbps maps 8 bits into one of the possible 256 symbols. The details of the modulation can be found in [5]. The data bits are mapped into the sequence c composed of 8 chips, where

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$$c = \{e^{j(f_1+f_2+f_3+f_4)}, e^{j(f_1+f_3+f_4)}, e^{j(f_1+f_2+f_4)},$$
$$-e^{j(f_1+f_4)}, e^{j(f_1+f_2+f_3)}, e^{j(f_1+f_3)}, -e^{j(f_1+f_2)}, e^{j(f_1)}\}$$

where the f_i's are generated from the (4 or 8) data bits using some form of differential QPSK modulation. To demodulate a CCK symbol, in principle, we have to correlate each received 8 chips with all possible (256 or 16) CCK sequences, and then choose as the demodulated sequence the one corresponding to the largest correlation. This correlation is practically infeasible. However, there exist techniques, such as the Walsh-Hadamard transform, whereby this correlation is simplified.

The frame of the 802.11b has a preamble during which a receiver can acquire the signal, achieve timing and frequency synchronization and estimate the channel taps between the transmitter and the receiver. If an LMS trained equalizer is to be used in the receiver, the equalizer taps can be trained using the preamble as well. The 802.11b standard provides for two preamble options, both using the 1 Mbps modulation rate. The short preamble has 72 barker sequences, while the long preamble has 144 barker sequences. When designing a receiver, one has to assume that all synchronization and estimation operations required should be done within the short preamble period.

The channel model typically encountered in the WLAN indoor environments is the exponential Rayleigh fading channel represented by a number of taps, each of which has a Rayleigh distribution. The zero delayed path is at the highest average power and the average power of the following paths decreases exponentially. In this channel model, the total power of all the paths is normalized to one for every channel realization. This channel is represented by

$$h_k = N(0, \tfrac{1}{2}s_k^2) + jN(0, \tfrac{1}{2}s_k^2), \; s_k^2 = s_0^2 e^{-kT_s/T_{rms}}$$
$$s_0^2 = 1 - e^{-T_s/T_{rms}}, \; \sum s_k^2 = 1$$

where h_k is the *i*th tap, T_s is the sampling interval, and T_{rms} is the delay spread of the channel. The number of paths depends on the delay spread assumed in the 802.11b environment. For a transmitter-receiver distance of 100 meters, a delay spread of 100 ns is usually assumed. The number of taps used should be no less than $10T_{RMS}/T_s$

III. Equalizer Training In CCK Modes

CCK sequences were designed to have low cross correlations, which leads to better performance in frequency selective channels than plain modulation techniques. Chips exist in the market that only use a rake receiver [1] for the reception of the 802.11b signals. However the performance of the rake receiver, which is just another name for the matched filter, is not adequate for high delay spreads in the neighborhood of 100 ns. Fig. 1 shows the performance of the 11 Mbps CCK mode when a perfect channel matched filter is used in the receiver compared to an AWGN environment. Also included is the ICI based DFE BER.

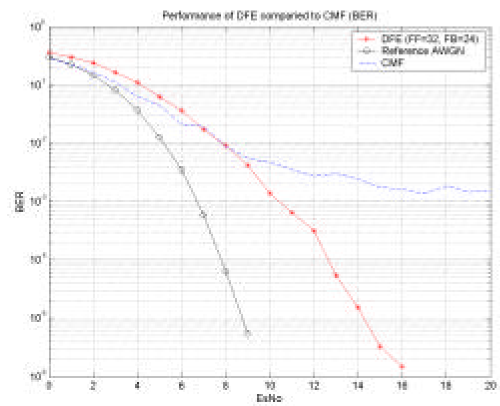

Fig. 1. BER for 11 Mbps CCK using channel matched filter

Fig. 1 shows that for the CCK 11 Mbps data rate, using only a matched filter exhibits an error floor at bit error rates higher than 10^{-3}. This corresponds to a packet error rate of about 0.4. Packet error rates are the important parameter to measure 802.11b performance since if a packet is in error it has to be retransmitted leading to wasted bandwidth. To mitigate such an unacceptable error floor, a DFE can be used. Since CCK is a modulation format that uses a sequence, a fundamental problem with the DFE occurs. To be able to obtain a decision on a CCK symbol, one has to feedback through the feedback filter of the DFE, *all* possible CCK sequences, one at a time. One would then correlate the output of the DFE feedforward section with the same sequence feedback, and after repeating for 256 times for the CCK 11 Mbps rate, the CCK demodulated sequence would be chosen as the one corresponding to the largest correlation as shown in [6]. Unfortunately, this technique is a computationally intensive technique, and the Walsh-Hadamard transform cannot be used. We will present two solutions to this problem.

A. *ICI based LS DFE*

A solution would be to use the DFE shown in Fig. 2, which can be called an ICI-based DFE. In this DFE one attempts to subtract the interchip interference via estimating each chip by itself using a hard decision decoding rather than using the sequence CCK decoder. Of course, one has to expect a loss when this DFE is used compared to the "optimal" DFE described before. This loss would be due to erroneous chip decisions that lead to error feedback. Several solutions exist to obtain the filter coefficients of the feedforward and feedbackward sections of the DFE equalizer. The optimal coefficients can be obtained using the technique outlined in [2]. In practice, one can obtain the coefficients using either a least squares (LS) or an adaptive least mean squares (LMS) solution. These are well known classical approaches [7]. The performance of the ICI-based DFE using LS training is shown in Fig. 3. Notice that because of error feedback, the performance loss for the ICI-based DFE is more than 6 dBs - from the performance of a DFE feeding back correct decisions- at high SNRs for the practical exponential channels.

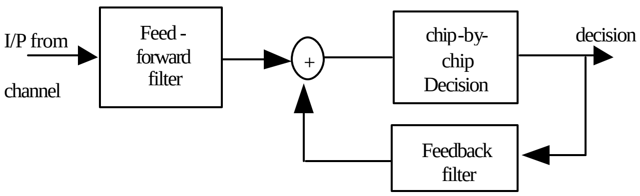

Fig. 2. ICI-based DFE system

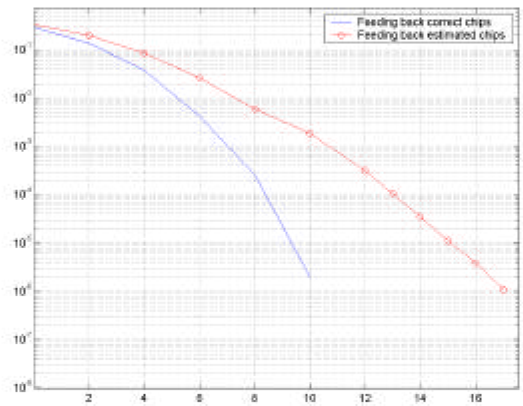

Fig. 3. BER for 11 Mbps CCK using chip DFE

To obtain the LS solution we represent the received sequence at time k by $r(k)$, then we can write:

$$r(k)=\sum h(k-l)x(l)+n(k)$$

where $r(k)$ are the received sequence samples at twice the chip rate (22 MHz in case of 802.11b), $x(k)$ are the chips (taken from a QPSK symbol set) at the chip rate (11 MHz in case of 802.11b), $h(k)$ is the convolution of the transmit filter and the channel, and $n(k)$ is the AWGN. The LS solution for the ICI-based DFE can be obtained from the least squares solution of the equation $\mathbf{AF}=\mathbf{Y}$, where $\mathbf{A}=[\mathbf{R}\,|\,\mathbf{X}]$, $\mathbf{R}$ is a matrix containing the received sequence values, and $\mathbf{X}$ is the input chips. Specifically,

$$\mathbf{A}=\begin{bmatrix} r(k) & r(k+1)\cdots & r(k+LFF\text{-}1) & | & \text{-}x(n) & \text{-}x(n+1)\cdots & \text{-}x(n+LFB-1) \\ r(k+2) & r(k+3)\cdots & r(k+LFF+1) & | & \text{-}x(n+1) & \text{-}x(n+2)\cdots & \text{-}x(n+LFB) \\ \vdots & \ddots & & | & & \ddots & \\ & \vdots & \vdots & | & \vdots & \vdots & \vdots \\ \vdots & & & | & & & \\ r(k+2*TL\text{-}2) & \cdots & \cdots r(k+LFF+2*TL\text{-}3) & | & \text{-}x(n+TL\text{-}1) & \cdots & \cdots\text{-}x(n+LFB+TL-2) \end{bmatrix}$$

F is the filter coefficients of the feedforward and feedbackward sections of the DFE equalizer, and can be written as

$$\mathbf{F}=\begin{bmatrix} FF(0) \\ \vdots \\ FF(LFF-1) \\ ------- \\ FB(0) \\ \vdots \\ FB(LFB-1) \end{bmatrix}$$

, Y is the training sequence, given by

$$\mathbf{Y}=\begin{bmatrix} x(n+LFB) \\ x(n+LFB+1) \\ \vdots \\ x(n+LFB+TL-1) \end{bmatrix},$$

TL is the training sequence length, LFF is the feedforward filter length, LFB is the feedbackward filter length, and k and n are chosen after synchronization such that we can deduce $x(n+LFB)$ from the vector $[r(k)\,r(k+1)\ \cdots r(k+LFF-1)]$. The LS solution to the equation $\mathbf{AF}=\mathbf{Y}$ can be written as

$$\mathbf{F}=\left(\mathbf{A}^T\mathbf{A}\right)^{-1}\mathbf{A}^T\mathbf{Y}\cdot$$

B. ISI based LS DFE

The second solution to the computational complexity of the conventional DFE is the ISI-based DFE. The ISI-based DFE feeds back chips only at symbol edges, i.e. after a symbol decision was taken as shown in Fig. 4. Notice that although this proposal is similar to previous proposals in the literature [3], previous proposals used an estimate of the channel impulse response as a feedback filter for the ISI-based DFE. Here, we will present a novel technique for obtaining the coefficients of the ISI-based DFE.

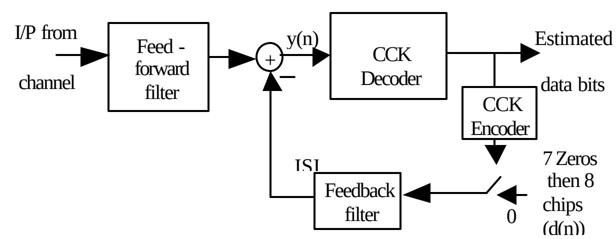

Fig. 4. ISI-based DFE system

We first have to note that we cannot use the same training technique of the ICI-based DFE for the ISI-based DFE, as can be deduced from Fig. 5. Our training technique relies on the fact that when we feedback CCK symbols only at the edges of each symbol, we are effectively feeding back zeros within each symbol. Hence our training algorithm has to account for that phenomenon.

In case of ISI-based DFE, we have to put zeros in the matrix $\mathbf{X}$ in place of chip decisions for 7 consecutive rows and then in the eighth row we place the chip decisions for the 8 chips. Note that during data reception, these chip decisions are obtained from the symbol decision made by the CCK decoder. Without loss of generality, assume that $8<LFB<16$ then we can construct the $\mathbf{X}$ matrix,

$$\mathbf{X}=\begin{bmatrix} -x(n) & -x(n+1) & \cdots & -x(n+4) & -x(n+5) & \cdots & -x(n+LFB-2) & -x(n+LFB-1) \\ -x(n+1) & -x(n+2) & \cdots & -x(n+5) & & & -x(n+LFB-1) & 0 \\ -x(n+2) & \iddots & \iddots & -x(n+6) & & \iddots & 0 & 0 \\ -x(n+3) & \iddots & & -x(n+7) & & \iddots & 0 & 0 \\ \vdots & \vdots & \iddots & & & & \vdots & \vdots \\ \boxed{-x(n+7)}^{9th} & \boxed{-x(n+8)}^{9th} & \cdots & \boxed{-x(n+11)}^{9th} & \boxed{0}^{9th} & \cdots & \boxed{0}^{9th} & \boxed{0}^{9th} \\ -x(n+8) & -x(n+9) & \cdots & -x(n+12) & -x(n+13) & \cdots & -x(n+LFB+6) & -x(n+LFB+7) \\ -x(n+9) & -x(n+10) & \cdots & -x(n+13) & -x(n+14) & \cdots & -x(n+LFB+7) & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \iddots & \vdots & \vdots \\ -x(n+TL-1) & -x(n+TL) & \cdots & \cdots & \cdots & \cdots & \cdots & \vdots \end{bmatrix},$$

and solve $\mathbf{AF} = \mathbf{Y}$ in the least squares sense as before.

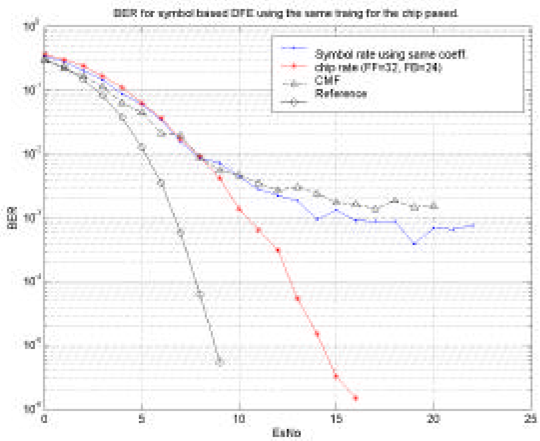

Fig. 5. BER for symbol based using same training in chip based at 11 Mbps

C. ISI based LMS DFE

When we use LMS training, we pass zeros into the feedback filter as opposed to passing the *known* (or estimated) training sequence. The ISI-based DFE LMS training is shown in Fig. 6

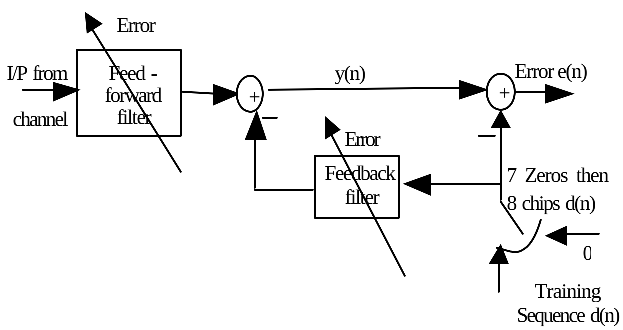

Fig. 6. LMS ISI-based DFE block diagram (during training)

IV. Simulation Results

Simulation results comparing the performance of the ISI and ICI DFEs are shown in Fig. 7 and Fig. 8. From Fig. 7, we can see that the ISI-DFE outperforms the ICI-DFE; although it has less complexity due to the fact that we feedback chip decisions into the feedback filter only at symbol edges, and in between symbol edges the feedback filter will have zeros. In case of LMS training both techniques have similar performance as shown in Fig. 8.

Notice that performance enhancements on the DFE can be obtained by employing more complex schemes involving several enhancements to the DFE equalizer, such as decision directed DFE, using longer training sequences, or feeding back correct decisions at symbol edges while using chip estimates within the symbol.

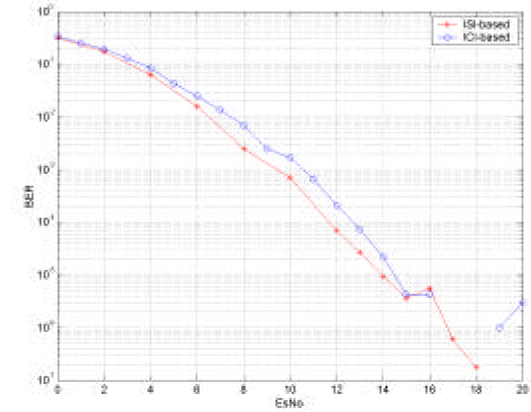

Fig. 7. BER performance for LS training

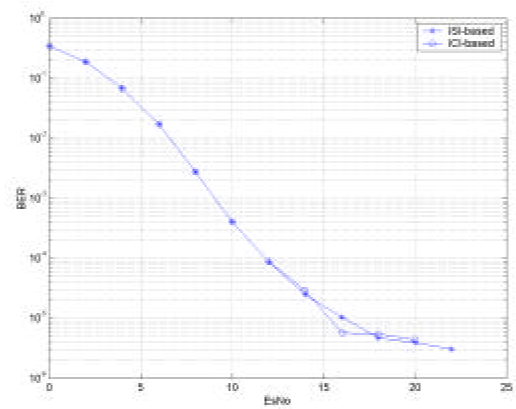

Fig. 8. BER performance for LMS training

V. Conclusion

We have presented a novel training algorithm for the ISI-based DFE that outperforms previously proposed training schemes for such equalizer. We have also shown that, although the ISI-based DFE obtained by the LS approach outperforms the ICI-based DFE obtained by the LS approach, as well as the DFEs obtained by LMS training.

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